Islanding Detection for Inverter-Based DG Coupled With Frequency-Dependent Static Loads

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***Abstract*—Islanding detection is an essential protection requirement for distribution generation (DG). Antiislanding techniques for inverter-based DG are typically designed and tested on constant RLC loads and, hence, do not take into account frequency-dependent loads. In this paper, a new antiislanding technique, based on simultaneous P-f and Q-V droops, is designed and tested under different islanding conditions considering different load types. The behavior of frequency-dependent static loads during islanding operation is discussed. The developed antiislanding technique is designed to fully address the critical islanding cases with frequency-dependent static loads and RLC-based loads. The performance of the proposed method is tested to accommodate load switching disturbances and grid voltage distortions. Theoretical investigation coupled with intensive simulation results using the Matlab/Simulink software is presented to validate the performance of the proposed antiislanding technique. Unlike previously proposed methods, the results show that the proposed islanding detection method is robust to frequency-dependent loads and system disturbances.**

***Index Terms*—Frequency-dependent static loads, inverter-based distribution generation (DG), islanding detection, nondetection zone (NDZ).**

I. Introduction

INCREASED penetration of distributed generation (DG) in power grids is evident to meet the increasing load demand and promote renewable energy sources. The increased DG penetration increases the distribution system complexity and raises several concerns. Among the most important concerns is islanding. Islanding is a condition in which a portion of the distribution system is comprised of DG, and local loads remains energized while they are unintentionally isolated from the rest of the system. The isolation could be a result of fault occurrence on the main distribution feeder. The re-closer will reconnect the isolated part of the system after a certain time interval (set by the system operator). This action is unfavorable since it may cause damage to the distribution system. Consequently, islanding detection (antiislanding) becomes an important DG protection requirement and it is mandated by the IEEE Std. 929 and IEEE Std. 1547 [1], [2].

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Antiislanding methods are categorized into passive, active, and communication-based methods. Among these methods, active methods are superior and widely embedded in DG protection since a smaller nondetection zone (NDZ) with minimum expenses can be achieved. Active methods are based on the perturbation and observation concept. Deliberate disturbances are injected in the DG circuit (via its electronic control scheme) to detect islanding cases. Active methods include slide-mode frequency shift [3], active frequency drift, or active frequency bias [4], Sandia frequency shift (SFS) [5], and injecting disturbances in either the d-axis or q-axis current controllers [6], [7]. Recently, active antiislanding methods that are based on implementing Q-f and P-V droops have been proposed, respectively, in [8] and [9]. The antiislanding droop of these methods is chosen so that during islanding, the DG-load system becomes unstable, resulting in voltage or frequency deviations. The aforementioned active methods are designed to tackle islanding detection cases with constant RLC loads.

Typically, some loads on the distribution system could be frequency and/or voltage dependent. It has been proven that frequency-dependent static loads affect passive and active antiislanding methods [10], [11]. In [10], it has been shown that the NDZ of the over/under voltage protection and the over/under frequency protection (OVP/UVP and OFP/UFP) method is dependent on the load frequency dependence. Similarly, the performance of the SFS active method as well as the NDZ is affected by the load frequency dependence [11].

In this paper, an antiislanding technique is developed to address islanding cases with frequency-dependent loads. The method is tested under various islanding and nonislanding conditions. Two droops P-f and Q-V are designed to simultaneously drift active and reactive power commands in such a manner that creates an unstable postislanding operation. The proposed islanding detection method is tested under matched and closely matched conditions taking into account different load types. Intensive theoretical analysis and simulation results, in the Matlab/Simulink environment, are conducted to validate the performance of the proposed antiislanding technique.

This paper is organized as follows. Section II presents the configuration of the system under study and addresses the representation of frequency-dependent static loads. Section III highlights the behavior of islanding detection methods in the presence of frequency-dependent static loads. The proposed antiislanding technique is discussed in Section IV. Simulation results and discussions are given in Section V, and, finally, conclusions are drawn in Section VI.

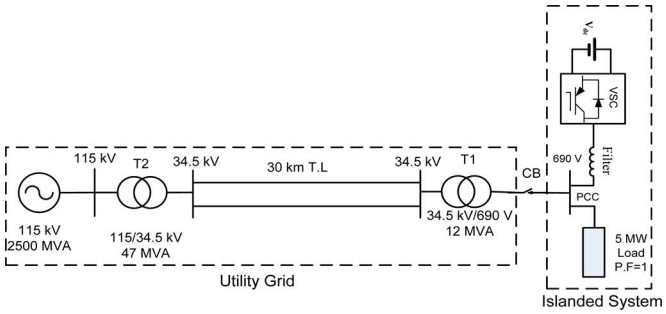

Fig. 1. Single-line diagram for the system under study.

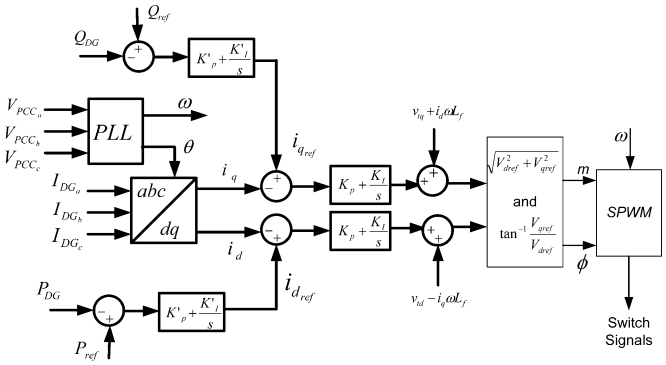

Fig. 2. Inverter control scheme based on the constant P&Q concept.

II. System Overview

A. Layout Description

The inverter-based DG under study (5 MVA) is connected to the grid transmission level via a radial link as shown in the single-line diagram in Fig. 1. A local load of 5 MW operating at the unity power factor is connected to the system at the point of common coupling (PCC). The DG/system data and system base quantities are given in Appendix A.

During an islanding condition, the circuit breaker (CB), shown in Fig. 1, isolates the DG and the local load from the whole system. If the active and reactive power rating of the load is equal or closely matches the DG active and reactive power output, the voltage and frequency variations will be within the standard permissible levels and, thus, the island will maintain stable operation. This unplanned islanding operation is unfavorable, since it may cause power-quality (PQ) problems, interference with grid protection devices, and personnel safety hazards. In this paper, the DG interface control is equipped with P-f and Q-V droops so that the DG becomes unstable once islanded. Different local load types and system operating conditions will be conducted to validate the proposed antiislanding technique.

The inverter control scheme, used in this paper, is based on the standard constant active and reactive power control and is shown in Fig. 2. Inputs of this control are the active and reactive power commands $P_{\rm ref}$ and $Q_{\rm ref}$, respectively. The output is the inverter voltage vector to be synthesized by a synchronized pulsewidth modulation (SPWM) module. Voltages at the PCC and inverter currents are taken as control feedbacks. The position and rotational speed of the voltage vector at the PCC is attained by a phase-locked loop (PLL) unit. Park transformation is used to represent the voltages and currents of the DG in a synchronous d–q frame and, thus, facilitates the decoupled control of the active and reactive power. A detailed description of the control scheme is presented in [12].

B. Static Load Representation

Different formulas were presented in the literature for static load representation [13]–[17]. To determine the parameters included in load representation formulas, measuring devices are installed at load terminals to track the load active and reactive power variation as a consequence to voltage and frequency deviations during a disturbance event. The load active power is expressed in terms of the voltage by a typical equation, described in the following form [14]:

$$P = P_0 \left(\frac{V}{V_0}\right)^{\rm np}. \tag{1}$$

Two or more terms with different exponents could be included in the load power/voltage relation. In order to include the frequency dependency effect in the static load representation, a frequency-dependency factor is multiplied by polynomial terms. This factor is typically expressed as follows:

$$(1 + k_{\rm pf}(f - f_0)) \tag{2}$$

where $k_{\rm pf}$ is the active power frequency dependency factor, ΔP(in per unit)/Δf (in per unit).

Typical static load representation, including voltage and frequency dependency, was used in the EPRI LOADSYN program [17]. This representation can be mathematically described as follows:

$$P = P_0 \left(a_1 \left(\frac{V}{V_0}\right)^{np1} + a_2 \left(\frac{V}{V_0}\right)^{np2} (1 + k_{\rm pf}(f - f_0))\right) \tag{3}$$

where $a_1 + a_2 = 1$, a_2 is the penetration ratio of frequency-dependent loads, and $np1$ and $np2$ are active power voltage dependency exponents.

III. Antiislanding Performance of P-V Droop with Frequency-Dependent Static Loads

Different active antiislanding methods have been designed to detect islanding for inverter-based DG with constant RLC loads. The method proposed in this paper relies on the droop concept. Recently, in [8] and [9], a single droop antiislanding concept has been developed but was not tested for frequency-dependent loads. For brevity, in this section, the P-V droop concept for islanding detection will be investigated taking into account frequency-dependent loads. The impact of frequency-dependent loads on the antiislanding capability of another conventional method, which is the SFS method, is discussed in Appendix B.

A P-V droop ($P_{\rm ref} = 2V - 1$) has been designed in [9] to facilitate islanding detection. As in other active antiislanding

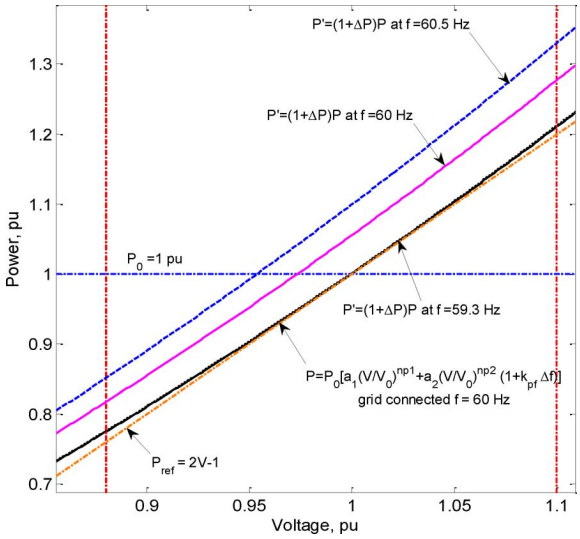

Fig. 3. Frequency effect on P-V curves of frequency-dependent loads at a positive mismatched case.

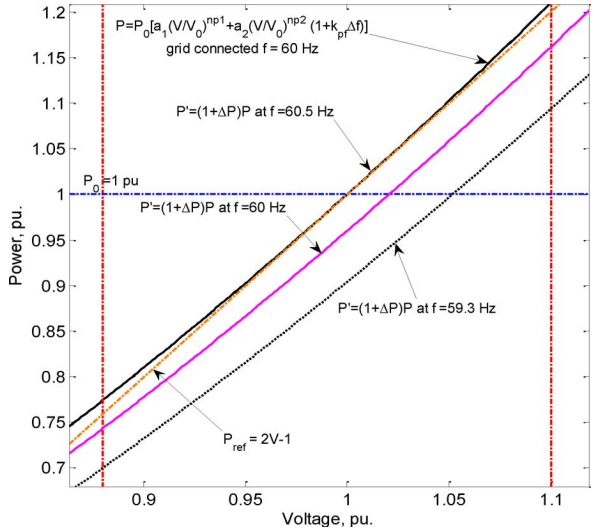

Fig. 4. Frequency effect on P-V curves of frequency-dependent loads at a negative mismatched case.

methods, the P-V droop technique is not designed to address islanding cases with frequency-dependent static loads. In the RLC case, voltage deviations are due to active power mismatches, while frequency deviations during islanding conditions are a result of reactive power mismatches. Thus, active and reactive power mismatches are decoupled for constant RLC loads during an islanding condition. With frequency-dependent loads, the active power mismatch becomes dependent on frequency deviations and, consequently, on reactive power mismatches.

The active power mismatch could be defined as the difference between the load active power and the DG active power (at nominal voltage and frequency values). Fig. 3 shows the effect of the active power load frequency dependence on the load curves for a positive active power mismatch condition. The load nominal values, illustrated in Fig. 3, are$P_0 = 1$ p.u., $V_0 = 1$ p.u., and $f_0 = 1$ p.u. (60 Hz). The active power mismatch (ΔP) is 0.055 p.u. and the reactive power mismatch (ΔQ) is tuned to give different frequency deviations, $-0.7, 0$, and 0.5 Hz. The load active power voltage dependency exponents *np1* and *np2* are assumed to be 2. The values of a_2, and $k_{\rm pf}$ are 1 and 5, respectively. As shown in Fig. 3, the load curve $P' = (1+\Delta P)P@f = 60$ Hz, drifts up or down depending on the amount of frequency deviation (-0.7 up-to 0.5 Hz). For a positive frequency deviation, the load curve will shift and become more distant from the P-V droop. This action makes islanding detection much easier (no intersection between the load and DG droop curve). Conversely, a negative frequency deviation, resulting from an islanding condition, will shift the load curve to become closer to the antiislanding P-V droop. Depending on the amount of frequency deviation, the shifted load curve might become tangential to the droop curve, as illustrated in Fig. 3. Hence, the islanded system will stabilize at $P = P_0 = 1$ p.u., and $V = V_0 = 1$ p.u. and, thus, islanding will not be detected.

Fig. 4 shows the shifting effect of the active power frequency-dependence parameter on a negative active power mismatch case. Unlike positive active power mismatch cases, the load curve shifts further away from the droop curve and, thus, facilitates islanding detection. It can be noted that although the load and droop curves might intersect (refer to Fig. 4), the intersection point is considered an unstable operating point [9]. On the contrary, positive frequency deviation will drift the load curves toward the antiislanding DG droop curve. Undetectable islanding conditions are likely to occur if the antiislanding droop is tangential to the shifted load P-V curves. The values of $(a_2, k_{\rm pf})$ are equal to (1, 5) while ΔP is set equal to -0.04 p.u.

The following mathematical analysis provides a criterion to address the islanding cases which are undetectable by the antiislanding droop. The frequency-dependent P-V load curve (P') can be expressed mathematically as follows:

$$P' = (P_0 + \Delta P)\left(a_1\left(\frac{V}{V_0}\right)^{np1} + a_2\left(\frac{V}{V_0}\right)^{np2}(1 + k_{\rm pf}(f - f_0))\right). \quad (4)$$

It can be seen from before that the worst undetectable islanding case occurs when the load curve is tangential to the DG droop at nominal voltage and power. For a zero active and reactive power mismatch condition, the P-V load curve (P) can be written as follows:

$$P = P_0\left(a_1\left(\frac{V}{V_0}\right)^{np1} + a_2\left(\frac{V}{V_0}\right)^{np2}\right). \quad (5)$$

An undetectable islanding case occurs when P' coincides with P at $V = V_0$

$$P' = P|_{V=V_0}. \quad (6)$$

Then

$$(P_0 + \Delta P)(a_1 + a_2(1 + k_{\rm pf}(f - f_0))) = P_0(a_1 + a_2). \quad (7)$$

Substituting $a_1 = 1 - a_2$ and $\Delta f = f - f_0$

$$\Delta P(1 - a_2 + a_2(1 + k_{\rm pf}\Delta f)) + P_0 \cdot a_2 \cdot k_{\rm pf}\Delta f = 0. \quad (8)$$

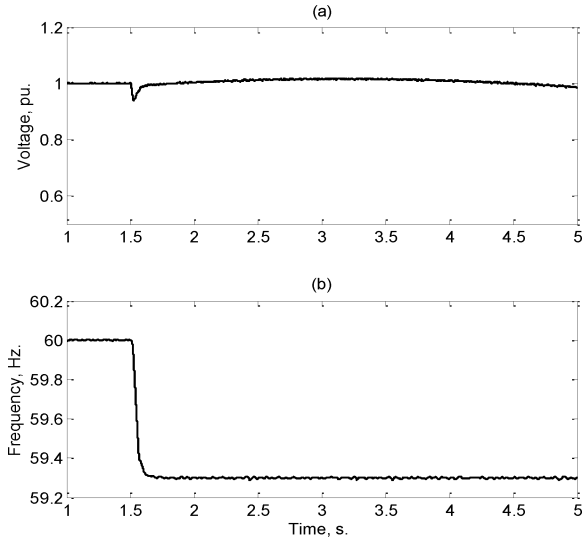

Fig. 5. Response of antiislanding droop $P_{\rm ref} = 2V - 1$ to an islanding case including overloaded frequency-dependent loads. (a) Voltage at PCC. (b) Islanded system frequency.

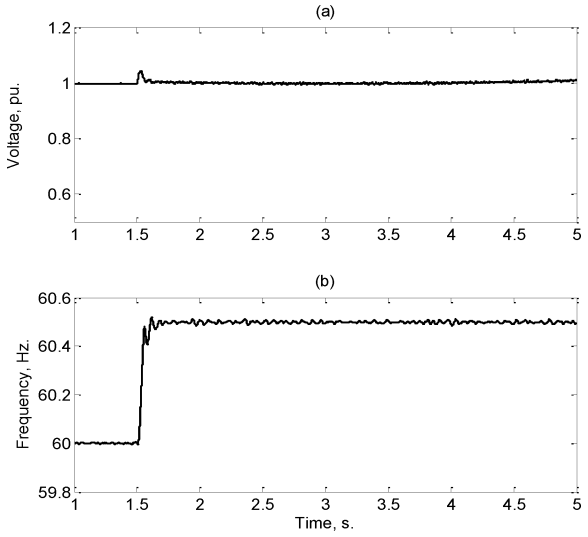

Fig. 6. Response of antiislanding droop $P_{\rm ref} = 2V - 1$ to an islanding case including underloaded frequency-dependent loads. (a) Voltage at PCC. (b) Islanded system frequency.

By mathematical manipulation, (8) is reduced to be

$$\Delta P(1 + a_2 \cdot k_{\rm pf}\Delta f) + P_0 \cdot a_2 \cdot k_{\rm pf}\Delta f = 0. \tag{9}$$

Equation (9) can be rewritten as follows:

$$a_2 \cdot k_{\rm pf}\Delta f = -\frac{\Delta P}{P_0 + \Delta P} \tag{10}$$

where Δf is the permissible frequency deviation and can range between -0.7/60 and 0.5/60 p.u. The load active power frequency-dependence parameter $k_{\rm pf}$ is a positive value and it could reach up to 5 for certain load types [11]. For constant RLC loads, $k_{\rm pf} = 0$ and, thus, the condition in (10) cannot be fulfilled unless $\Delta P = 0$ (i.e., islanding cases with zero active power mismatch are the only undetectable cases for the P-V antiislanding droop curve).

For frequency-dependent static loads, $k_{\rm pf} \neq 0$ and $a_2 \neq 0$. Hence, there is an unlimited number of loading cases that satisfy the condition in (10), for which the P-V antiislanding droop would fail to detect islanding. When ΔP is positive, a negative Δf, resulting from a negative ΔQ, could generate undetectable cases. From (10), some of the possible unlimited combinations of ΔP and Δf that are undetectable include (0.055, -0.7/60), (0.04, -0.46/60), and (0.03, -0.35/60) for the case where $k_{\rm pf} = 5$ and $a_2 = 1$. Vice versa, for islanding cases with frequency-dependent loads and experiencing negative ΔP, positive frequency deviations may result in undetectable cases. Similarly, by referring to (10), unlimited combinations of ΔP and Δf, could result in undetectable islanding conditions; for example, (-0.04, 0.5/60), (-0.03, 0.37/60), and (-0.02, 0.24/60).

Two islanding cases of an inverter-based DG with two different frequency-dependent static loads have been simulated to validate the aforementioned mathematical analysis. The system under study, shown in Fig. 1, is simulated in the Matlab/Simulink environment. Operation and load parameters for the first case are tuned to fulfill the condition expressed in (10), $P_0 = 1$ p.u., $\Delta P = 0.055$ p.u., $a_2 = 1, k_{\rm pf} = 5$, and $\Delta Q = -0.023$ p.u. (which will result in a $\Delta f = 0.7$/60 p.u.). The load-quality factor (Q_f) is assumed to be 1. Voltage and frequency variations are shown in Fig. 5 where an islanding action (by switching off CB) is initiated at $t = 1.5$ s. As shown in Fig. 5(a), the voltage momentarily drops at the instant of islanding, and then it resumes preislanding conditions and, thus, islanding will not be detected. The frequency drops to its lower threshold limit (59.3 Hz) due to the reactive power mismatch, which is not sufficient to operate the frequency relays.

The parameters for the second islanding case are $P_0 = 1$ p.u., $a_2 = 1, k_{\rm pf} = 5, Q_f = 1, \Delta P = -0.04$ p.u. and $\Delta Q = 0.017$ p.u. Voltage and frequency variations are shown in Fig. 6. As depicted in Fig. 6, the antiislanding droop fails to disturb the islanded system since the voltage stabilizes at 1 p.u. [Fig. 6(a)] and the frequency settles at the upper frequency limit 60.5 Hz, as shown in Fig. 6(b). Thus, loads with active power frequency dependence can affect the P-V droop performance, resulting in undetectable islanding cases.

Since the analysis in this paper focuses on the load active power frequency-dependency effect, the voltage dependency exponents *np1* and *np2* are set equal to 2, which is the worst case from the antiislanding prospective.

IV. Proposed Antiislanding Technique

In this section, a new antiislanding method is proposed. It is based on the droop concept and takes into account the drawbacks of previously developed droop approaches with frequency-dependent loads. Irrespective of the load type, load parameters or the kind of mismatch (active or reactive power) that is experienced during islanding, the new technique is designed to have the full capability to detect different islanding cases and avoid false actions caused by transient disturbances. The proposed antiislanding technique is based on constructing two simultaneous P–f and Q–V droops. The general form of $P_{\rm ref}$ is represented as follows:

$$P_{\rm ref} = A \cdot \Delta f + P_0 \tag{11}$$

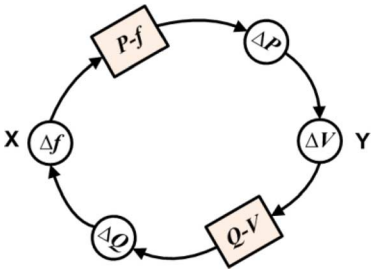

Fig. 7. Schematic description of the proposed antiislanding technique.

where

A slope of the $P-f$ droop;

Δf frequency deviation $\Delta f = f - f_0$ (in per unit).

The grid code recommendation for the DG reactive power setting is to operate at zero reactive power exchange at the PCC, which is known as unity power factor setting [18]. Hence, the Q-V droop is mathematically defined as follows:

$$Q_{\text{ref}} = B \cdot \Delta V \tag{12}$$

where

B slope of the Q-V droop;

ΔV the voltage deviation $\Delta V = V - V_0$ (in per unit).

Load parameters and DG/load active and reactive power mismatches affect the antiislanding performance of the P-f and Q-V droops. Typically, a negative slope for the P-f and Q-V droops is used to maintain intentional islanded stable operation [19]. This concept should be avoided for systems, where islanding detection is a mandate. The magnitudes of the slopes should be selected in such a way that facilitates islanding detection under different operating conditions. Directions of the P-f and Q-V droops are designed according to the voltage and frequency deviations. Once a permissible voltage or frequency deviation is detected, a predefined short time delay (50 ms) will be applied to examine the directions of voltage and frequency drifts and accordingly predict the proper steering for the droops. Given the absolute slope values and droop directions, P-f and Q-V droops are created and activated.

The proposed antiislanding technique depends on incremental and parallel degradation in frequency and voltage values. Frequency and voltage deviations are amplified in a cyclic manner to hit the frequency or voltage thresholds of either the OFP/UFP or the OVP/UVP, respectively. The strategy of the proposed antiislanding technique is described in Fig. 7.

Consider an islanding case with a frequency deviation and zero voltage deviation. Starting from point X, shown in Fig. 7, the frequency deviation will reallocate the reference power command, by the action of the implemented P-f droop, from (P_0) to $(A \cdot \Delta f + P_0)$. A new active power settling point will emerge and, consequently, a voltage drift will appear. Based on the developed Q-V droop, the voltage deviation will move the reference reactive power command from $(Q_{\text{ref}} = 0)$ to $(Q_{\text{ref}} = B \cdot \Delta V)$. Shifting the DG reactive power command will result in a new reactive power settling point and, thus, results in accumulating frequency deviation. This sequence is reiterated until either the OFP/UFP or the OVP/UVP is triggered.

The sequence, shown in Fig. 7, can be represented mathematically in the following set of equations. In order to illustrate the mechanism of the proposed antiislanding technique, an islanding case, including a reactive power mismatch and a zero active power mismatch, is considered. By referring to point X, a frequency deviation will result from a reactive power mismatch which can be expressed as follows [10]:

$$\Delta f = f_0 \left(\sqrt{1 + \frac{\Delta Q}{Q_0}} - 1 \right) \tag{13}$$

where

Q_0 load capacitive reactive power;

ΔQ reactive power mismatch $\Delta Q = Q_{\text{load}} - Q_{\text{DG}}$.

Initially, $Q_{\text{DG}} = 0$, then $\Delta Q = Q_{\text{load}} = Q_l - Q_0$, where Q_l is the load inductive reactive power. Based on the frequency deviation, the active power command can be expressed as

$$P_{\text{ref}} = P_0 + A \cdot f_0 \left(\sqrt{1 + \frac{\Delta Q}{Q_0}} - 1 \right). \tag{14}$$

During islanding, since the DG is the sole source, the DG power equates to the load active power to determine the amount of voltage deviation as follows:

$$P_0 + A \cdot \Delta f = (P_0 + \Delta P)(1 + a_2 \cdot k_{\text{pf}} \Delta f) \left(\frac{V}{V_0} \right)^2 \tag{15}$$

$$V = V_0 \sqrt{\frac{P_0 + A \cdot \Delta f}{(P_0 + \Delta P)(1 + a_2 \cdot k_{\text{pf}} \Delta f)}} \tag{16}$$

$$\begin{aligned} \Delta V &= V - V_0 \\ &= V_0 \left(\sqrt{\frac{P_0 + A \cdot \Delta f}{(P_0 + \Delta P)(1 + a_2 \cdot k_{\text{pf}} \Delta f)}} - 1 \right). \end{aligned} \tag{17}$$

Consequently, with the voltage deviation shown before, the reference reactive power command will change as follows:

$$\begin{aligned} Q_{\text{ref}} &= B \cdot \Delta V \\ &= B \cdot V_0 \left(\sqrt{\frac{P_0 + A \cdot \Delta f}{(P_0 + \Delta P)(1 + a_2 \cdot k_{\text{pf}} \Delta f)}} - 1 \right). \end{aligned} \tag{18}$$

Hence, the reactive mismatch after one cycle ΔQ^1 is

$$\Delta Q^1 = \Delta Q - B \cdot V_0 \times \left(\sqrt{\frac{P_0 + A \cdot \Delta f}{(P_0 + \Delta P)(1 + a_2 \cdot k_{\text{pf}} \Delta f)}} - 1 \right). \tag{19}$$

From (13), Δf will be positive when ΔQ is positive and vice-versa. In order to ensure that the frequency and voltage will diverge continuously, $|\Delta Q^1|$ should be greater than $|\Delta Q|$. According to (19), in order to fulfill this condition, slopes A and B should have different signs.

Referring to (17), ΔV could settle at the zero level and, thus, will stop the sequence of deterioration. This condition occurs when

$$P_0 + A \cdot \Delta f = (P_0 + \Delta P)(1 + a_2 \cdot k_{\rm pf} \Delta f). \quad (20)$$

The term $a_2 \cdot k_{\rm pf}$, seen in (20), is always positive. In order to avoid the condition shown in (20), the value of A should be a negative value. As explained in (19), the slopes A and B should have different signs; and, hence, B should be a positive value. Based on the magnified reactive power mismatch ΔQ^1, the frequency deviation after one cycle (Δf^1) becomes larger than Δf. This sequence of frequency and voltage deterioration is automatically repeated to activate DG protection.

A different islanding case with a local load, including an active power mismatch (ΔP) and a zero reactive power mismatch, is mathematically investigated. In this case, Δf is initially equal to zero and, hence, point Y shown in Fig. 7 will be the starting point. Since $\Delta Q = 0$, and $Q_{\rm DG}$ is initially set to zero, then $Q_l - Q_0 = 0$. The active power mismatch is defined as

$$\Delta P = P_{\rm load} - P_0. \quad (21)$$

The voltage deviation caused by the active power mismatch is given as follows:

$$\Delta V = V_0 \left(\sqrt{\frac{P_0}{P_0 + \Delta P}} - 1 \right). \quad (22)$$

Accordingly, the reference reactive power command is

$$Q_{\rm ref} = B \cdot V_0 \left(\sqrt{\frac{P_0}{P_0 + \Delta P}} - 1 \right). \quad (23)$$

By using (23), the reactive power mismatch can be expressed as follows:

$$\Delta Q = -Q_{\rm ref} = -B \cdot V_0 \left(\sqrt{\frac{P_0}{P_0 + \Delta P}} - 1 \right). \quad (24)$$

As a result of the reactive power mismatch, a frequency deviation arises

$$\Delta f = f_0 \left(\sqrt{1 - \frac{B \cdot \Delta V \cdot (1 + \Delta f / f_0)}{Q_0 (1 + \Delta V / V_0)^2}} - 1 \right). \quad (25)$$

Based on the frequency deviation, the active power command is modified as follows:

$$P_{\rm ref} = P_0 + A \cdot f_0 \left(\sqrt{1 - \frac{B \cdot \Delta V \cdot (1 + \Delta f / f_0)}{Q_0 (1 + \Delta V / V_0)^2}} - 1 \right). \quad (26)$$

Hence, the active mismatch after one cycle ΔP^1 is

$$\Delta P^1 = \Delta P - A \cdot f_0 \left(\sqrt{1 - \frac{B \cdot \Delta V \cdot (1 + \Delta f / f_0)}{Q_0 (1 + \Delta V / V_0)^2}} - 1 \right). \quad (27)$$

According to (22), ΔV will be positive if ΔP is negative and vice-versa. It is assumed that $f_0 \gg \Delta f$ and, hence, $(1 + \Delta f / f_0)$ is always positive. Similar to (19), in order to enforce the absolute of ΔP^1 being greater than the absolute of ΔP, the slopes A and B, should have different signs. As explained in (20), negative and positive slopes are, respectively, selected for the P-f and Q-V droops to ensure better antiislanding performance for islanding cases with frequency-dependent static loads.

Islanding cases that are initiated with frequency and voltage deviations require more attention. By applying the P-f and Q-V antiislanding droops, the voltage and frequency deviations are defined in (17) and (25), respectively. From (17) and (25), the voltage deviation is affected by the frequency deviation and vice-versa. With unplanned implementation of the antiislanding P-f and Q-V droops, the voltage and frequency deviations may restrain each other and, hence, be within the permissible region, which will adversely affect islanding detection.

Depending on the incident voltage and frequency deviations, the directions of the antiislanding P-f and Q - V droops, A and B, will be adjusted as follows:

$$\text{sign}(A) = \text{sign}(\Delta f \cdot \Delta V) \quad (28)$$

$$\text{sign}(B) = -\text{sign}(A). \quad (29)$$

The strategy employed for adjusting directions of the droops can be described in the flowchart, illustrated in Fig. 8. The step-by-step procedure illustrates the operation of the proposed method as follows.

Step 1) Detect voltage and frequency deviations.

Step 2) If the voltage and/or frequency exceed(s) their limits, the DG will be tripped; otherwise, proceed to the following step.

Step 3) Apply a 50-ms time delay from detection to correctly determine the direction of the voltage and frequency deviations.

Step 4) Determine the directions of the droops, based on the flowchart given in Fig. 8.

Step 5) Given the absolute slopes of the droops and their directions, create the P-f and Q-V droops.

Islanding cases with small active or reactive power mismatches require steeper droops compared to islanding cases with large active and reactive power mismatches. In order to facilitate islanding detection under different conditions, particularly matched and closely matched conditions, the absolute slope values of the P-f and Q-V droops, A and B, are selected to be 15 and 0.2, respectively. Note that the frequency deviation Δf is taken in per units, (the base value, $f_0 = 60$ Hz). Steeper P-f and Q-V droops could be more effective in islanding detection; however, the antiislanding technique may become very sensitive to other transient events occurrning nearby in the distribution system. The favorable features of the proposed antiislanding technique, based on the parallel operation of the P-f and Q-V droops, are summarized as follows:

- accommodating RLC and frequency-dependent static loads with different parameters;
- proper performance with load switching disturbances and grid voltage distortions;

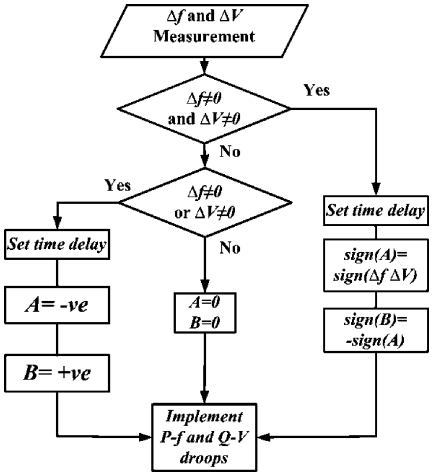

Fig. 8. Steering strategy of the antiislanding P-f and Q-V droops.

- easy to be implemented since there is no change in the inner current control loops.

It is worthy to note that the droop steering is dependent on the initial deviations of the voltage and frequency at the instant of islanding. In rare islanding cases, the voltage and/or frequency deviations momentarily start in a certain direction then change and resume in a different direction. Therefore, sufficient time delay should be set to correctly determine the directions of voltage and frequency deviations. The time delay here is set at 50 ms to accommodate all cases of islanding. A shorter time delay is favorable, but it could result in unsatisfactory performance with some cases of islanding. Thus, there is a tradeoff between reducing the time delay and the performance of the islanding detection method.

V. Simulation Results and Discussion

In this section, several simulation results, using Matlab/Simulink software, are carried out to ensure the effectiveness and feasibility of the proposed antiislanding technique under different load types and operating conditions. The system under study is described by the single-line diagram in Fig. 1. The following subsections will present the response of the proposed antiislanding technique to different inverter-based DG islanding conditions and system disturbances.

A. Performance of the Proposed Antiislanding Technique Compared to the P-V Droop Islanding Detection Method

In this subsection, the proposed algorithm, explained in Section IV, will be tested against the critical islanding cases that are unsuccessfully detected by the droop $P_{\text{ref}} = 2V - 1$ (refer to Section III). The parameters of the two islanding cases, previously discussed with the droop, $P_{\text{ref}} = 2V - 1$, are shown in Table I.

Fig. 9 shows voltage and frequency deviations for the two cases as a result of an islanding occurrence at $t = 1.5$ s, where the proposed antiislanding is employed. As can be seen from Fig. 9, islanding is detected since the frequency in both cases exceeds the permissible frequency limits within approximately 100 ms (including the predefined time delay). The voltage in both cases also drifts beyond its limits, which confirms the antiislanding tripping action.

TABLE I
Operational and Load Parameters for the Islanding Cases Under Study

Case	a_2	k_{pf}	$np1$	$np2$	Q_f	P_0	ΔP	ΔQ
#1	1	5	2	2	1	1	0.055	-0.023
#2	1	5	2	2	1	1	-0.04	0.017

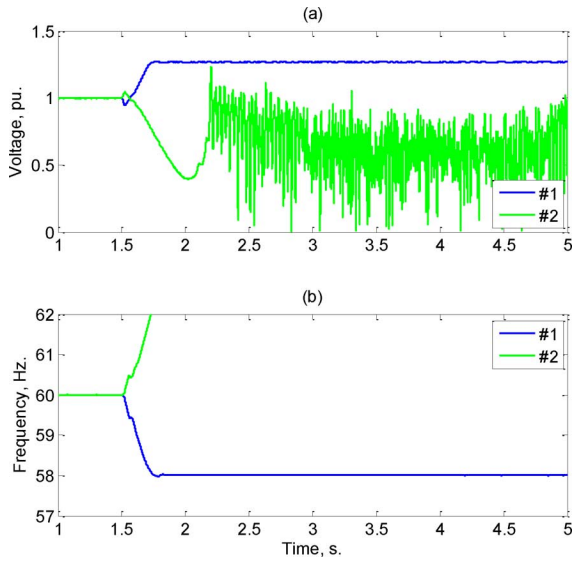

Fig. 9. Proposed antiislanding technique versus islanding cases with frequency-dependent static loads. (a) Voltage at the PCC. (b) Islanded system frequency.

B. Performance of the Proposed Antiislanding Technique With Matched and Closely Matched Islanding Cases

In this subsection, the proposed technique is examined for islanding cases including RLC loads with and without slightly reactive power mismatches of -1% and 1%. This kind of testing, described in [20], is based on the UL 1741 Standard. It examines the response of the antiislanding technique to matched and closely matched islanding cases with different adjustable active power ratings: 0.25, 0.5, 1, 1.25 p.u. For brevity, in the islanding cases under study, the DG active power is set at 1 p.u., and the load active power is adjusted to match the DG power $\Delta P = 0$. The load-quality factor of the load is assumed to be 1.

Three islanding cases have been simulated with active and reactive power mismatches of $(\Delta P = 0, \Delta Q = -1\%), (\Delta P = 0, \Delta Q = 1\%)$, and $(\Delta P = 0, \Delta Q = 0)$. Fig. 10 shows the voltage and frequency deviations resulting from the three islanding cases. The three islanding cases are detected by the proposed algorithm since the frequency deviations of the three cases, shown in Fig. 10(b), exceed the permissible frequency limits (59.3–60.5 Hz) within the 2-s margin, recommended in the IEEE Std. 1547 [2]. Voltage variations for the three cases also deviate beyond the permissible region (0.88–1.1 p.u.), indicated by the horizontal dashed lines in Fig. 10(a).

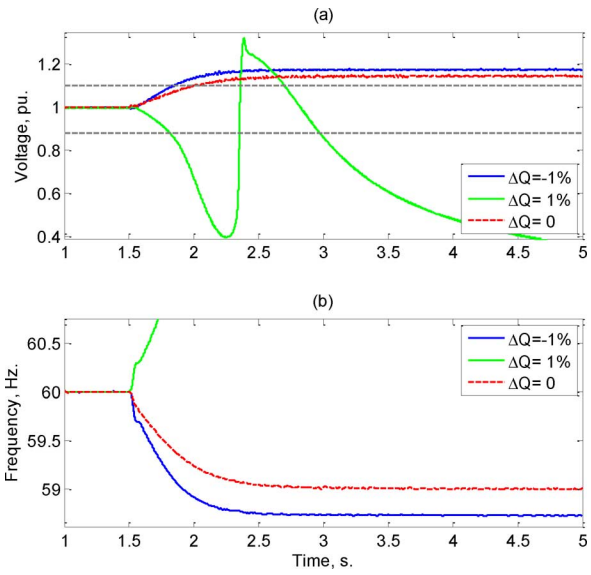

Fig. 10. Response of the proposed antiislanding technique to islanding events with matched and closely matched conditions ($\Delta P = 0$). (a) Voltage at PCC. (b) Islanded system frequency.

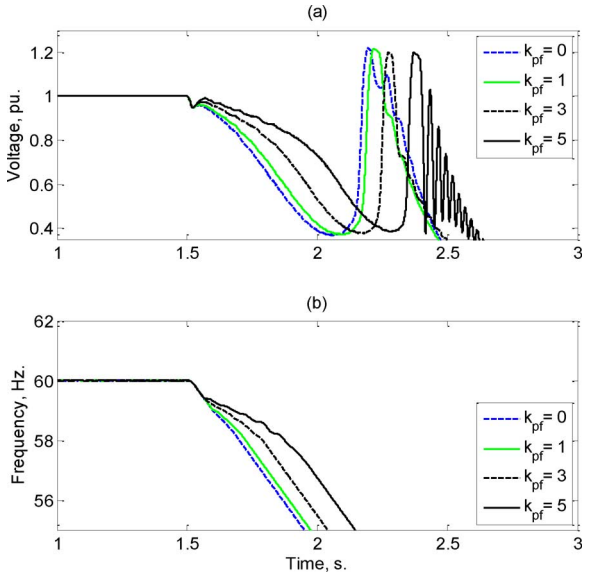

Fig. 11. Impact of different load frequency-dependence parameters on the proposed antiislanding method. (a) Voltage at PCC. (b) Islanded system frequency.

TABLE II
OPERATIONAL AND LOAD PARAMETERS FOR ISLANDING CASES WITH DIFFERENT $k_{\rm pf}$ VALUES

Case	a_2	k_{pf}	$np1$	$np2$	Q_f	P_0	ΔP	ΔQ
#1	1	0	2	2	1	1	0.05	-0.02
#2	1	1	2	2	1	1	0.05	-0.02
#3	1	3	2	2	1	1	0.05	-0.02
#4	1	5	2	2	1	1	0.05	-0.02

C. Response to Different Values of the Load Frequency-Dependence Parameter $(k_{\rm pf})$

This subsection investigates the performance of the proposed method for different values of the load active power frequency dependency parameter $(k_{\rm pf})$. Four islanding cases with different $k_{\rm pf}$ values, described in Table II, are simulated to examine the proposed algorithm when different frequency-dependent loads are experienced.

Fig. 11 describes the voltage and frequency variations of the four islanding cases when the proposed method is applied. As shown in Fig. 11, the voltage and frequency deviations exceed the IEEE standard limits [2]. The trend of voltage and frequency variations for nonzero $k_{\rm pf}$ values, 1, 3, and 5, is almost the same. It can be seen that frequency and voltage variations (Fig. 11) for islanding cases with smaller frequency-dependence parameters rapidly exceed the permissible limits.

D. Response to Different Load Quality Factors (Q_f)

The load-quality factor (Q_f) can be defined mathematically as follows:

$$Q_f = \frac{Q_0}{P_0} \tag{30}$$

where Q_0 is the load capacitive reactive power and P_0 is the load active power at nominal voltage and frequency values.

TABLE III
OPERATIONAL AND LOAD PARAMETERS FOR ISLANDING CASES WITH DIFFERENT LOAD-QUALITY FACTORS

Case	a_2	k_{pf}	$np1$	$np2$	Q_f	P_0	ΔP	ΔQ
#1	1	1	2	2	1	1	0.05	-0.02
#2	1	1	2	2	2	1	0.05	-0.02
#3	1	1	2	2	4	1	0.05	-0.02

In this subsection, the performance of the proposed antiislanding technique is tested under different load-quality factors. Three islanding cases with different load-quality factors, described in Table III, are simulated.

Fig. 12 describes the voltage and frequency variations of the three islanding cases when the proposed technique is implemented. As shown in Fig. 12, the voltage and frequency waveforms increase beyond their limits. As the quality factors increase, the amount of frequency deviation decreases during islanding operation [Fig. 12(b)]. The proposed algorithm is capable of detecting islanding for loads with a quality factor Q_f up to 4.

E. Response to Load Switching at the PCC

As a result of transient grid disturbances, sensitive antiislanding methods might be activated and, thus, erroneously enforce the DG to disconnect. The impact of this interfering depends on many issues, such as disturbance type and location, DG penetration level, grid stiffness, and antiislanding sensitivity. Load switching events is one reason why antiislanding maloperation [21] could occur.

This subsection examines the performance of the proposed technique when load switching events occurred in a given power system, shown in Fig. 1. In this test procedure, an extra load of 1 p.u. with unity power factor and unity quality factor is switched in and out at the PCC at 1.5 and 3.5 s, respectively. Fig. 13 presents the voltage and frequency variations as a consequence to load switching. From Fig. 13, it can be seen that the voltage and frequency variations of both cases, with and without antiislanding

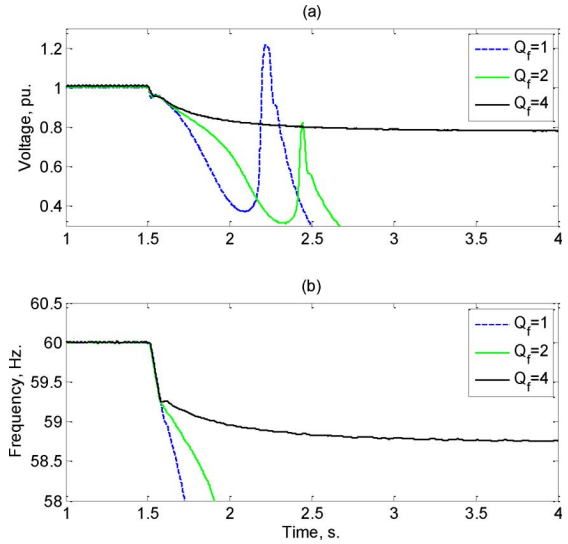

Fig. 12. Antiislanding performance at different load-quality factors. (a) Voltage at PCC. (b) Islanded system frequency.

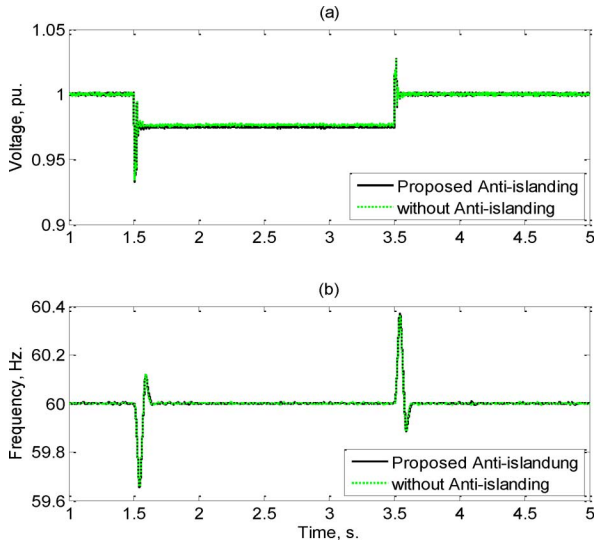

Fig. 13. Response of the proposed antiislanding technique to load switching at PCC; (a) Voltage at the PCC. (b) Islanded system frequency.

technique, totally coincide (i.e., the proposed algorithm has a negligible effect on the system behavior during load switching).

F. Performance of the Proposed Antiislanding Technique With Voltage Harmonic Content and Voltage Unbalance

Among issues that could affect the performance of the antiislanding methods are voltage harmonics and grid voltage unbalance. Antiislanding techniques may fail to detect certain islanding conditions due to the existence of voltage harmonics and voltage unbalance. Further, during grid-connected operation, antiislanding techniques could be unnecessarily activated due to the interference with voltage harmonics and voltage unbalance, thus leading to false DG tripping.

In this subsection, the antiislanding algorithm is tested against voltage harmonics and voltage unbalance conditions. Two islanding cases are simulated to investigate both issues and for both cases $\Delta P = 0.05$ p.u., $\Delta Q = -0.02$ p.u., $Q_f = 1$, and $k_{\rm pf} = 0$.

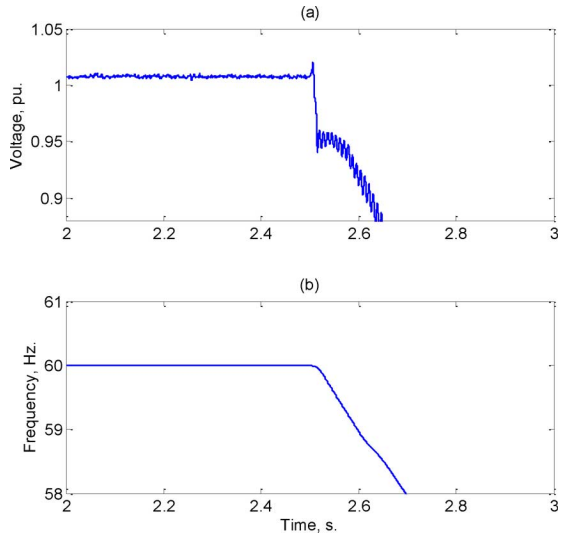

Fig. 14. Performance of the proposed antiislanding technique with a $\mathrm{THD_v} \approx 10.5\%$ (islanded at $t = 2.5$ s). (a) Voltage at the PCC. (b) Islanded system frequency.

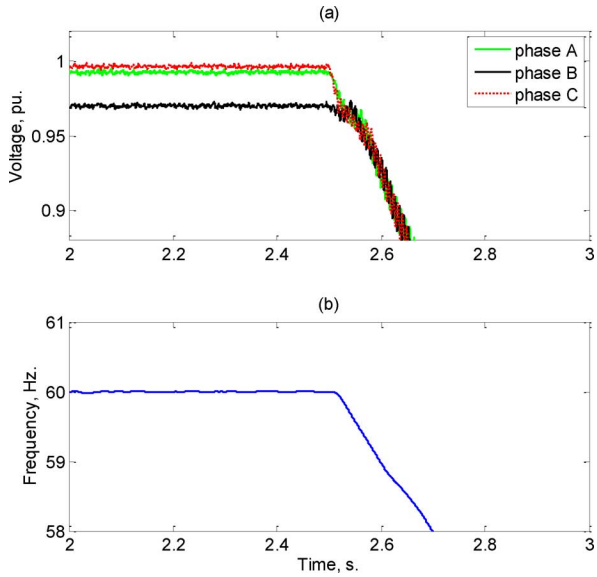

Fig. 15. Performance of the proposed antiislanding technique with voltage unbalance (islanded at $t = 2.5$ s.). (a) Phase voltages at PCC. (b) Islanded system frequency.

The first islanding case addresses the impact of voltage harmonics. In this case, second- and third-order voltage harmonics of 7% each are imposed on the grid equivalent voltage source and, hence, the total voltage harmonic distortion $(\mathrm{THD_v})$ at the PCC increases from 2.4% to around 10.5%. Fig. 14 describes the voltage and frequency variations during an islanding occurrence at $t = 2.5$ s. It can be seen that the proposed technique properly detects the islanding condition, as shown in Fig. 14. Moreover, it does not adversely interfere with voltage harmonics during grid-connected operation, prior to $t = 2.5$ s.

The other islanding case is to examine the antiislanding method during system unbalance. At the grid equivalent voltage source, a 5% reduction on the amplitude of phase A is applied to demonstrate a voltage unbalance condition. Fig. 15 illustrates the phase voltages at the PCC and frequency variations during an islanding event at $t = 2.5$ s. As can be seen in Fig. 15, frequency

and phase voltages deviate beyond their respective permissible margins as islanding occurs (i.e., the antiislanding technique is capable of detecting islanding conditions). For $t < 2.5$ s, rms phase voltages, shown in Fig. 15(a), are at different levels, and the antiislanding technique does not interfere with the DG operation during grid-connected operation.

VI. Conclusion

This paper presents a new antiislanding technique capable of detecting islanding with frequency-dependent loads. The proposed technique is independent of load parameters and is based on an emerging chain of frequency and voltage deteriorations once an islanding condition occurs. The antiislanding technique relies on a set of simultaneous P-f/Q-V droops. The droops are designed according to the directions of the incident voltage and frequency deviations at the instant of islanding. Based on simulation results, the proposed algorithm is capable of detecting islanding cases that include frequency-dependent static loads. Loads with different frequency-dependency parameters and different quality factors are considered. The proposed method complies with the islanding detection tests provided in the IEEE Standard 1547 and UL 1741. Further, the algorithm has been tested against system disturbances and voltage distortions (load switching, voltage harmonics, and voltage unbalance) and it has been shown that the antiislanding performance is not adversely affected. Theoretical study, along with simulation results, confirms that the proposed antiislanding technique is a feasible and reliable solution for inverter-based DG with frequency-dependent loads.

Appendix A

- *Inverter based DG*
  nominal power: 5 MVA;
  nominal dc voltage: 1440 V;
  nominal ac voltage (LL): 690 V;
  nominal frequency: 60 Hz.;
  inverter rating: 1.2 p.u.;
  filter impedance: j0.3 p.u.
- *Data for each transmission line of the two parallel lines:*
  length: 30 km;
  positive- and zero-sequence resistances: 0.1153, 0.413 Ω/km;
  positive- and zero-sequence inductances: 1.05, 3.32 mH/km;
  positive- and zero-sequence capacitances: 11.33, 5.01 nF/km.
- *Transformer T1:*
  nominal power: 12 MVA;
  nominal frequency: 60 Hz;
  ratio: 34.5 kV/690 V, Yg/Δ.
  HV winding:
  voltage (LL): 34.5 kV;
  resistance and inductance: 0.00083, 0.025 p.u.
  LV winding:
  voltage (LL): 690 V;
  resistance and inductance: 0.00083, 0.025 p.u.;
  magnetization resistance and reactance: 500, 500 p.u.

TABLE IV
Base and Rated Quantities for the System Under Study

Quantity	*Value*
Base Power	5 MVA
Base voltage at the PCC	690 V
Base frequency	60 Hz

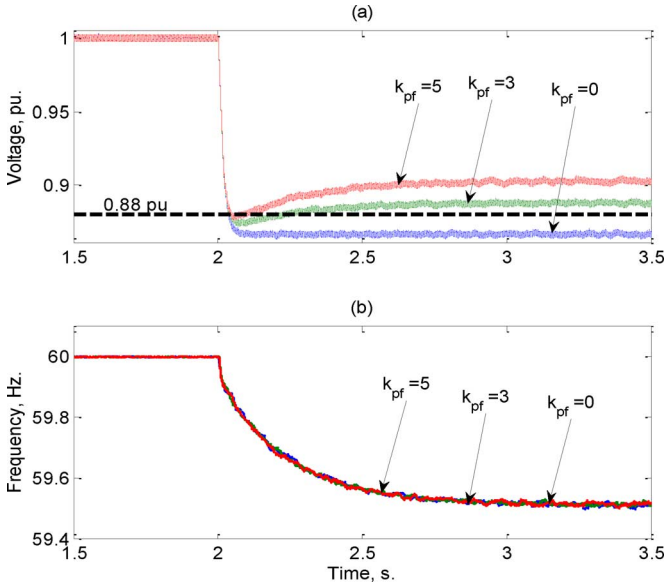

Fig. 16. Performance of the SFS method for the case where $\Delta P = 0.15$ p.u., and $\Delta Q = -0.02$ p.u. (islanded at $t = 2$ s.). (a) Voltage at PCC. (b): Islanded system frequency.

- *Transformer T2:*
  nominal power: 47 MVA;
  nominal frequency: 60 Hz;
  ratio 115 kV/34.5 kV, Yg/Δ.
  HV winding:
  voltage (LL): 115 kV;
  resistance and inductance: 0.00267, 0.08 p.u.
  LV winding:
  voltage (LL): 34.5 kV;
  Resistance and inductance: 0.00267, 0.08 p.u.;
  Magnetization resistance and reactance: 500, 500 p.u.

Appendix B

In this Appendix, the impact of the load frequency dependency parameter on the performance of the SFS antiislanding method is examined. An islanding condition takes place at $t = 2$ s for a load with $\Delta P = 0.15$ p.u., $\Delta Q = -0.02$ p.u., and $Q_f = 1.5$. The parameters of the SFS method, defined in [11], are $cf = 0$, and $k = 0.005$. The SFS method is tested for different $k_{\rm pf}$ values (0, 3, and 5). Voltage and frequency deviations, for the described islanding case, are shown in Fig. 16. It can be seen that the SFS method is capable of detecting the islanding condition in the presence of RLC loads ($k_{\rm pf} = 0$). However, with frequency-dependent loads ($k_{\rm pf} = 3$ or $k_{\rm pf} = 5$), the voltage and frequency stabilize at a value that is within the voltage and frequency relay standard levels. It can be seen that load frequency dependency has an impact on the performance of the SFS method.

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